REMARKS

Claims 1-10 were examined. Claims 1 and 2 were rejected and Claims 3-10 were objected to. In response to the above-identified Office Action, Applicants decline to amend any claims. No claims are canceled, and no new claims are added. Reconsideration of the rejected claims in light of the aforementioned amendments and the following remarks is requested.

I. Claims Rejected Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1 and 2 under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,938,196 issued to Richardson et al. ("*Richardson*"). Although *Richardson* is closely related art, Applicants believe it fails to teach or suggest at least one aspect of the present invention as recited in claim 1, and for at least that reason will ask the Examiner to withdraw these rejections.

Claim 1 recites a message-passing decoder comprising several elements, including a check node function unit for calculating a parity check message, wherein the parity check message corresponding to a logic function output for an input from a bit node function unit is calculated according to a linear approximation function determined for each divided interval of the logic function. The "linear approximation function determined for each divided interval" is shown in Figure 5, and may also be described as a piecewise linear approximation (the line segments 520 connecting points 521 approximate the continuous function shown as dashed line 510). As the Examiner notes, *Richardson* lacks the claimed linear approximation function. However, contrary to the Examiner's position, Applicants submit that the Examiner's proposed modification of *Richardson* would not be undertaken, because *Richardson* deals with the mathematical complexities of LDPC decoding differently. Specifically, *Richardson* uses the approximation $\ln(\coth(\frac{\delta x}{2})) \approx 2e^{-\delta x}$ (*see* [0059]) to simplify

calculations, and accordingly quantizes input values y to integer multiples of $\frac{\ln 2}{2}$ (*see* [0079]) before processing.

This is qualitatively different from Applicants' approach of calculating the parity check message corresponding to a logic function output according to a linear approximation function determined for each divided interval of the logic function. For at least this reason, Applicants respectfully submit that claim 1 is not obvious in view of *Richardson*, and request that the Examiner withdraw this rejection.

Claim 2 depends upon claim 1, and is believed to be patentable for at least the reason discussed above in support of that base claim. Applicants ask the Examiner to withdraw this rejection also.

II. Allowable Claims

Applicants note with appreciation that the Examiner found claims 3-10 objectionable for being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, in view of Applicants' foregoing remarks regarding the base claim of all of claims 3-10, Applicants believe those claims are allowable in their current form and request that the Examiner withdraw these objections.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-10, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

Dated: 7/28, 2006

Respectfully submitted,
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Katherine Jennings — 7-28-06

Katherine Jennings — Date